

**Amendments to the Drawings:**

The attached sheet of drawings includes changes to FIG. 2. This sheet replaces the original sheet including FIG. 2. In FIG. 2, the missing label CASCLK has been.

Attachment: Replacement Sheet

**REMARKS**

The Examiner objected to the drawings, stating "The drawings are objected to because in figure 2, a signal reference label "CASCLK" indicating a second column address strobe clock is omitted. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application." In response, Applicants have amended FIG. 2 to include the missing CASCLK label without adding new matter.

The Examiner has stated that claims 17-26 are allowed and claims 12-15 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter.

The Examiner rejected claim 11 under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent 6,434,082 to Hovis et al.

The Examiner rejected claim 16, stating "Claim 16 is rejected under 35 U.S.C §112, (second) paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The recitation "said first write recovery time" in line 5, should be --said second write recovery time-- for relating to the second clock frequency. Similarly, the recitation "said first time interval" in line 6 should read --said second time interval--. Also note that the second write recovery time is 12 nanoseconds, not 15 nanoseconds--." In response, Applicants have amended claim 16 as the Examiner has recommended.

Applicants respectfully traverse §102(e) rejections with the following arguments.

35 USC § 102

As to claim 11, the Examiner states that "Regarding claim 11, Hovis discloses an SDRAM comprising: at least one bank of DRAM cells (Background Art); said SDRAM operable to a first specification (PC100 in figure 2) defined by a first clock frequency (Clock Period = 10 ns), a first write recovery time ( $t_{WR}=20$  ns) and a first time interval for precharge to row address strobe ( $t_{RP}=30$  ns); and means (on-chip timer, column 6, line 20) for programming said SDRAM operable to a second specification (PC 133) defined by a second clock frequency (ClockPeriod = 7 ns), a second write recovery time ( $t_{WR}=14$  ns) and a second time interval for precharge to row address strobe ( $t_{RP}=21$  ns)."

Applicants contend that claim 11, as amended, is not anticipated by Hovis et al. because Hovis et al. does not teach each and every feature of claim 11. In a first example Hovis et al. does not teach "a programmable circuit adapted to control operation of said SDRAM based on said first and said second write recovery times." In a second example, Hovis et al. does not teach "operable to a second specification defined by a second clock frequency, a second write recovery time and a second time interval for precharge to row address strobe."

Applicants respectfully point out that Hovis et al. is teaching in col. 6, lines 19-23, a dynamic change of write recovery time over a range about a nominal write recovery time of a single SDRAM specification in response to variations caused by process, voltage and temperature variations affecting a timer circuit generating the write recovery time. The different write recovery times of Hovis et al. generated by the timer circuit are not different write recovery times of different SDRAM specifications but unwanted changes to the write recovery time. Hovis et al. indicates this by the statements in col. 6, lines 27 and 30 that "yield loss will result" at some of the write recovery times generated by the timer. Yield loss means not functional

to the specification.

Further, the timer circuit of Hovis et al. can not be considered a programmable circuit in the ordinary sense of the word or in the sense taught in Applicants specification there is no way to program the timer circuit for to generate a selected write recovery time during normal operation of any particular Hovis et al. SDRAM.

Still further, the write recovery time of Hovis et al. cannot be a function of "said first and said second write recovery times" of a first and a second SDRAM specification as Applicants claim requires since the timer circuit is designed to generate only a single write recovery time of a single SDRAM specification. The timer circuit of Hovis et al. has no knowledge of any other write recovery time specification other than the single write recovery time the timer circuit is designed to generate and thus it is not operable to two different SDRAM specifications having two different write recovery times.

Based on the preceding arguments, Applicants respectfully maintain that claim 11 is not unpatentable over Hovis et al. and is in condition for allowance. Since claims 27-31 depend from claim 11, Applicants respectfully maintain that claims 27-31 are likewise in condition for allowance.

**CONCLUSION**

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,  
FOR: Jacunski et al.

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